Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte YUKIO FUZISAWA, TAKEHIRO FURUKAWA, and TAKASHI YAMASAKI

Appeal No. 1998-3326
Application No. 08/498,819

ON BRIEF

Before BARRETT, RUGGIERO, and BARRY, Administrative Patent Judges.

BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the rejection of claims 1 and 3-10. We reverse.

BACKGROUND

The appellants' invention relates to "arbitration" and "arbitration judgement." Arbitration is the process of acquiring the right to transmit data via a data bus;

arbitration judgment is the process of comparing data on the bus with the

address of, for example, a microcomputer on the bus. Both processes require strict detection of a start bit across the bus. If such detection is delayed, arbitration judgment will not occur during the current machine cycle.

Software and hardware approaches have both been tried to detect the timing of a start bit issued by a microcomputer on a data bus. The software approach monitored a bus to detect when a start bit was issued thereon. Unfortunately, several machine cycles were required to detect the existence of the start bit on the bus, which resulted in late detection. The hardware approach enabled the output of data from a serial input-output (SIO) register by issuing a start bit to the register. Unfortunately, timing between the issuance of the start bit and a clock signal on the bus was asynchronous, which resulted in a clock pulse cycle delay from the issuance of the start bit until the output of data from the SIO register.

The appellants' microcomputer features a built-in SIO circuit. The SIO circuit uses a counter to count a basic input clock signal. Via switches and a gate, the counter supplies a transfer clock signal to an SIO register. Responsive to an external signal from another microcomputer on a data bus, an initialization circuit comprising flip-flops resets the counter. Because the initialization circuit immediately resets the counter in response to a change in the external signal, delay in detection of the start bit on the bus is decreased and timing between the microcomputers is synchronized.

Claim 9, which is representative for our purposes, follows:

> 9. A microcomputer comprising:
>
> a serial I/O register for performing data conversion;
>
> a built-in serial input-output circuit comprising a resettable counter for counting a basic clock signal and supplying a transfer clock signal to the serial input-output register; and
>
> flip-flop circuits responsive to an external signal for resetting said counter circuit.

The prior art applied in rejecting the claims follows:

Miyazaki	4,939,741	July 3, 1990
Okada et al. (Okada)	5,396,225	Mar. 7, 1995

Claims 1 and 3-10 stand rejected under 35 U.S.C. § 103 as being obvious over Miyazaki in view of Okada. Rather than reiterate the arguments of the appellants or examiner in toto, we refer the reader to the briefs and answer for the respective details thereof.

OPINION

In deciding this appeal, we considered the subject matter on appeal and the rejection of the examiner. Furthermore, we duly considered the arguments and evidence of the appellants and examiner. After considering the record, we are persuaded that the examiner erred in rejecting claims 1 and 3-10. Accordingly, we reverse.

We begin by noting the following principles from In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993).

> In rejecting claims under 35 U.S.C. Section 103, the examiner bears the initial burden of presenting a prima facie case of obviousness. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).... "A prima facie case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." In re Bell, 991 F.2d 781, 782, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting In re Rinehart, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)).

With these principles in mind, we consider the examiner's rejection and the appellants' argument.

The examiner asserts, "**Miyazaki** discloses an invention substantially as claimed, including a data processing ('DP') system comprising ... initializing means [column 4 (line 67) - column 5 (line 12)]". (Examiner's Answer at 3.) The appellants argue, “neither Miyazaki nor Okada et al. disclose or suggest the fundamental concept of initialization means resetting the counter in response to a signal from an external circuit." (Appeal Br. at 11.)

“‘[T]he main purpose of the examination, to which every application is subjected, is to try to make sure that what

each claim defines is patentable. [T]he name of the game is the claim ....'" In re Hiniker Co., 150 F.3d 1362, 1369, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998)(quoting Giles S. Rich, The Extent of the Protection and Interpretation of Claims--American Perspectives, 21 Int'l Rev. Indus. Prop. & Copyright L. 497, 499, 501 (1990)). Here, claims 1-8 specify in pertinent part the following limitations: "an initializing means for initializing said clock signal supply means responsive to a signal from an external circuit; wherein said clock supply means is a counter for counting a basic clock signal, and said initialization means
resets the counter responsive to a signal from the external circuit." Similarly, claim 9 specifies in pertinent part the following limitations: "flip-flop circuits responsive to an external signal for resetting said counter circuit." Also similarly, claim 10 specifies in pertinent part the following limitations: "an initialization circuit responsive to a receiving preparation completion signal from another microcomputer for resetting said counter." Accordingly, claims 1-10 require resetting a counter in response to an external signal.

The examiner fails to show a teaching or suggestion of the limitations in the prior art of record. "The examiner's position is that the Miyazaki's system would inherently reset the counter." (Paper No. 9). According to the appellants, "[t]he Examiner indicated during an in-person interview (Paper No. 9) that counter 24 inherently discloses a reset function. The Examiner argued that when the 3-bit counter 24 completes a count cycle, i.e. completes counting from 0-7, that the counter may be viewed as inherently 'resetting' back to zero." (Appeal Br. at 9.)

For its part, Miyazaki teaches a "3-bit counter **24**, which counts the clock RMV generated by the synchronization circuit **10**." Col. 4, l. 68, - col. 5, l. 2. Although the counter is reset, however, it is not reset in response to an external signal. To the contrary, the counter is reset after reaching the state 111 when it receives the next pulse of the clock RMV. Cf. Charles H. Roth, Fundamentals of Logic Design 268-69 (3d ed. 1085)("Note that when the counter reaches the state 111, the next pulse resets it to the 000 state

....")(copy attached). Relying on Okada only to teach "a serial input-output means for outputting data in converting parallel data into serial data and for converting an input serial data into parallel data[,]" (Examiner's Answer at 4), the examiner fails to allege, let alone show, that the reference cures the deficiency of Miyazaki.

Because Miyazaki's counter is not reset in response to an external signal, we are not persuaded that teachings from the prior art would have suggested the limitations of "an initializing means for initializing said clock signal supply means responsive to a signal from an external circuit; wherein said clock supply means is a counter for counting a basic clock signal, and said initialization means resets the counter responsive to a signal from the external circuit[;]" "flip-flop circuits responsive to an external signal for resetting said counter circuit[;]" or "an initialization circuit responsive to a receiving preparation completion signal from another microcomputer for resetting said counter." Therefore, we reverse the rejection of claims 1 and 3-10 as being obvious over Miyazaki in view of Okada.

CONCLUSION

In summary, the rejection of claims 1 and 3-10 under § 103 is reversed.

REVERSED

LEE E. BARRETT Administrative Patent Judge	)
JOSEPH F. RUGGIERO Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
LANCE LEONARD BARRY Administrative Patent Judge	)

LLB/KIS

MCDERMOTT, WILL & EMERY
600 13TH STREET, NW
WASHINGTON, DC 20005